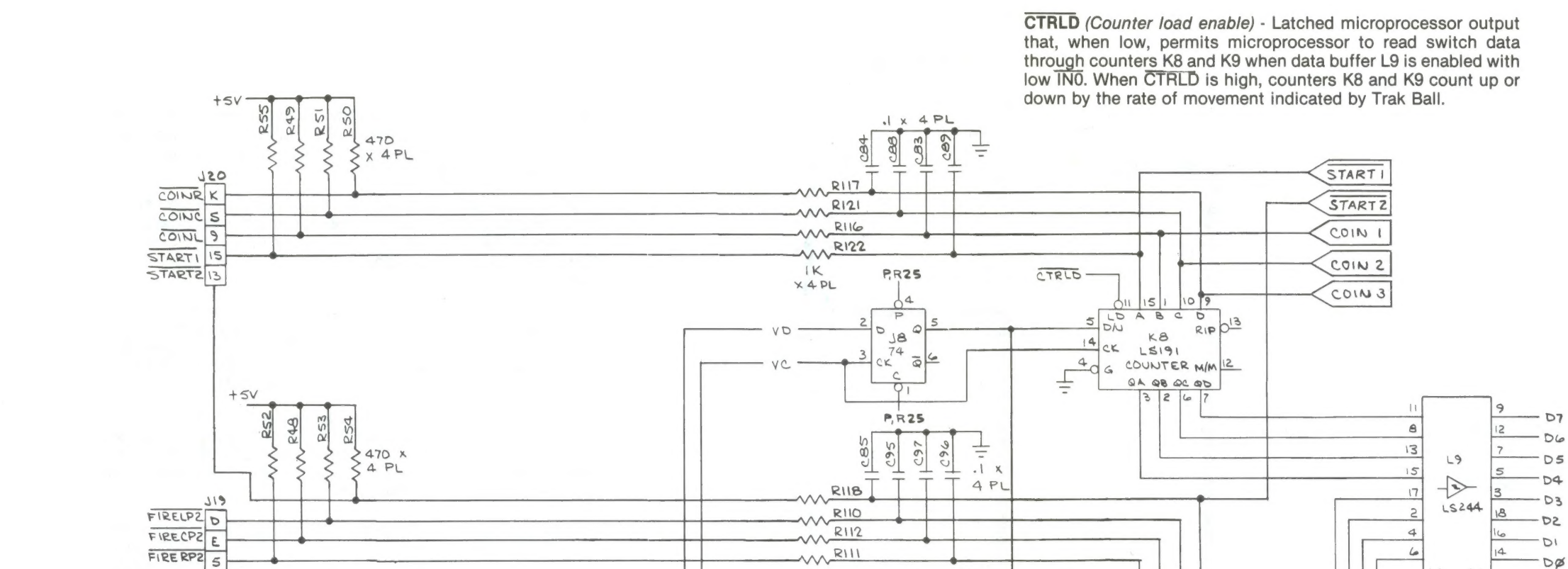
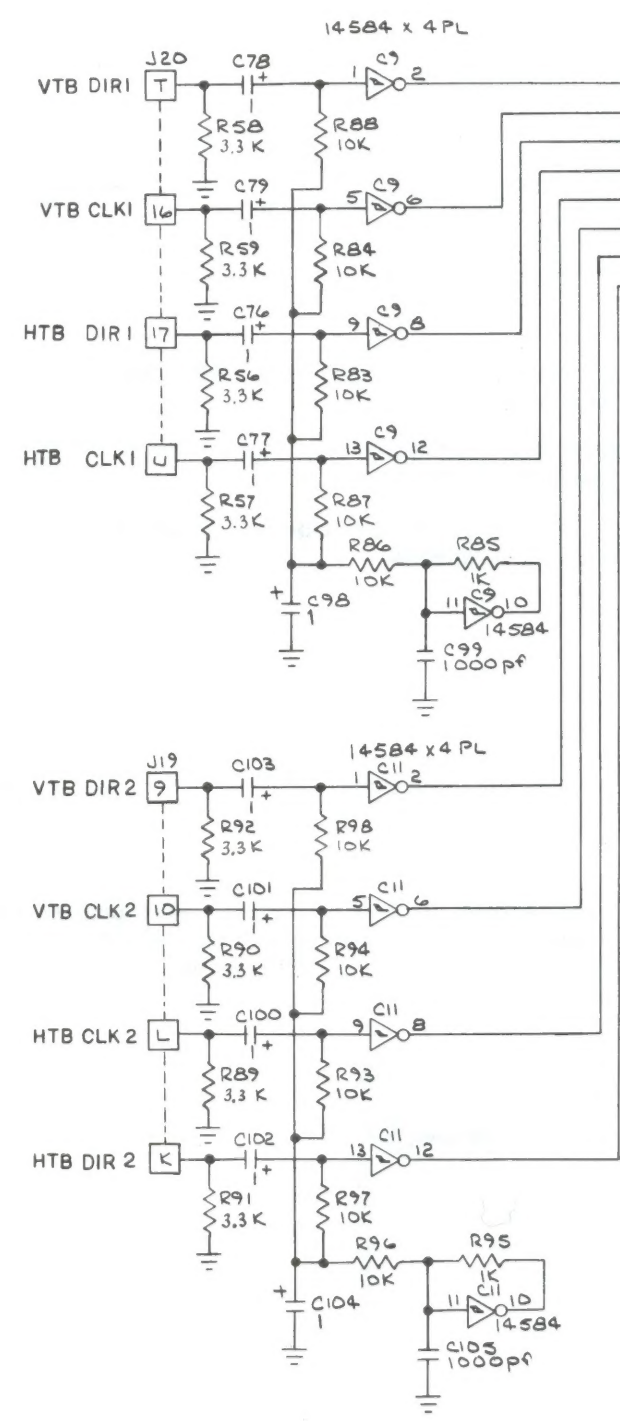


Input Circuits



FLIP - Microprocessor-generated signal that reverses the horizontal rate of movement (HTBCLK2) and direction (HTBDIR2) of second player's Trak Ball input on Missile Command Cocktail game. Cocktail game must have -02 or higher Program Memory installed.



CTRLD (*Counter load enable*) - Latched microprocessor output that, when low, permits microprocessor to read switch data through counters K8 and K9 when data buffer L9 is enabled with low **IN0**. When **CTRLD** is high, counters K8 and K9 count up or down by the rate of movement indicated by Trak Ball.

VC (Trak Ball Vertical Clock) - Clock output of multiplexer D9 that originates in the vertical steering PCB of the Trak Ball, used to clock flip-flop J8 and counter K8. If VC leads VD, then K8 counts down. If it lags HD, then K8 counts up.

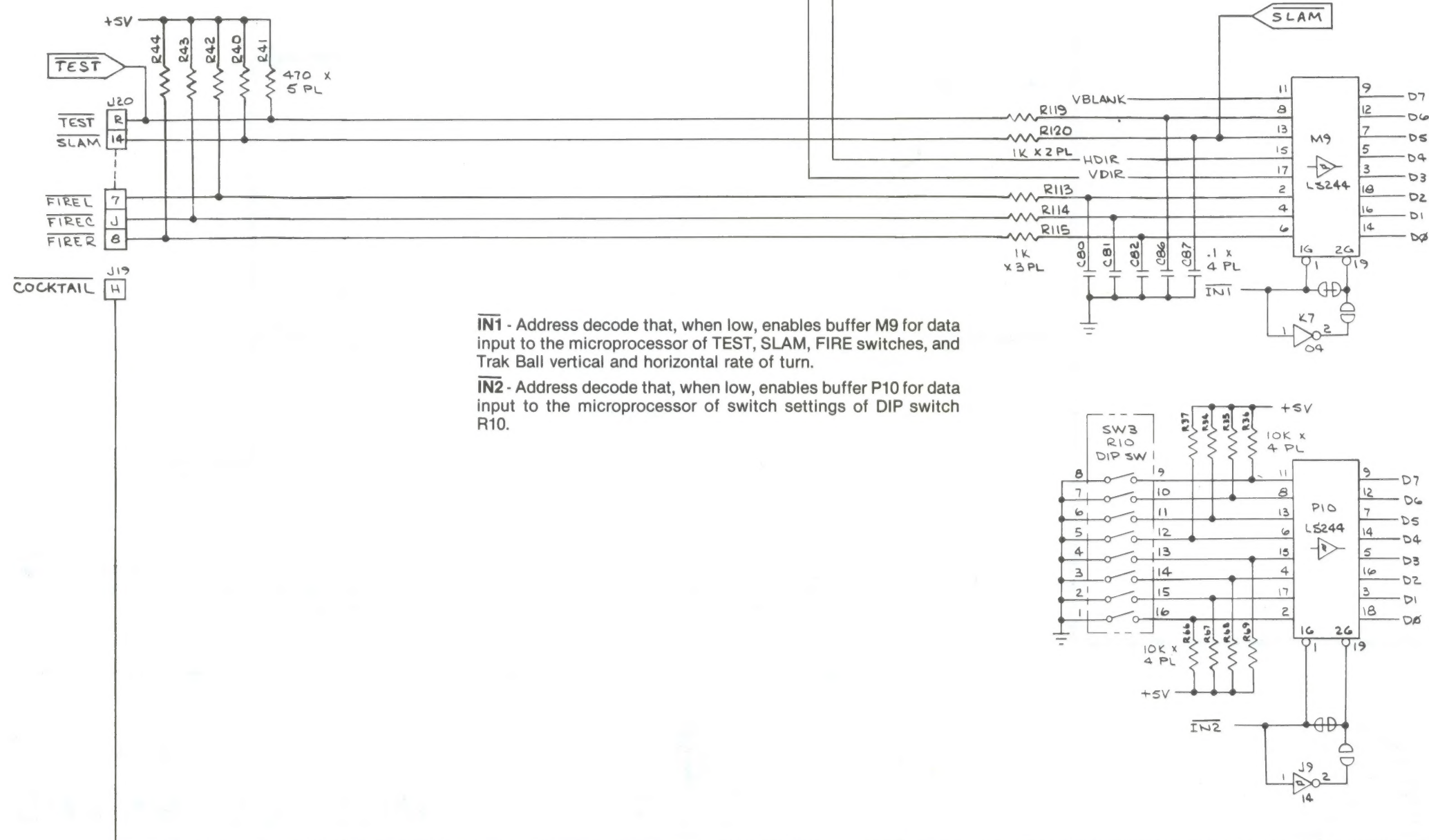
VD (Trak Ball Vertical Direction) - Direction output of multiplexer D9 that originates in vertical steering PCB of Trak Ball. See VC description.

HC (Trak Ball Horizontal Clock) - Clock output multiplexer D9 that originates in the horizontal steering PCB of the Trak Ball, used to clock flip-flop J8 and counter K9. If HC leads HD, then K9 counts down. If it leads HD, then K9 counts up.

HD (Trak Ball Horizontal Direction) - Direction output of multiplexer D9 that originates in horizontal steering PCB of Trak Ball. See HC description.

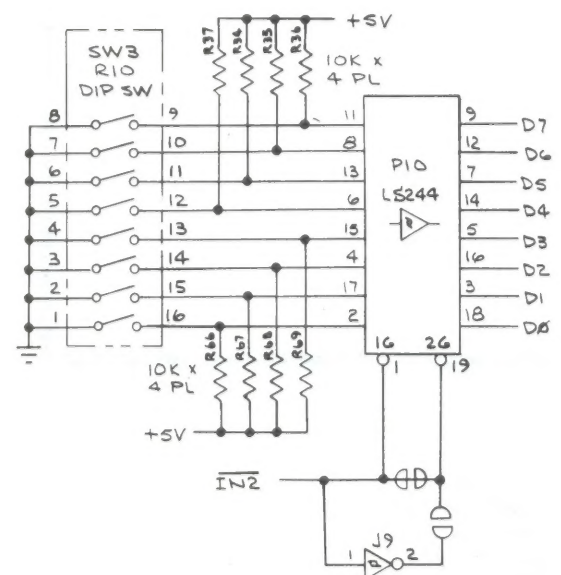
HTBCLKX (*Horizontal Trak Ball Clock*) - Player 1 or player 2 horizontal Trak Ball clock input to game PCB from horizontal steering PCB of Trak Ball. Player 2 input is used only in a Cocktail game, and game PCB must have -02 or higher Program Memory installed.

HTBDIRX (*Horizontal Trak Ball Direction*) - Player 1 or player 2 horizontal Trak Ball direction input to game PCB from horizontal steering PCB of Trak Ball. Player 2 input is used only in a Cocktail game, and game PCB must have -02 or higher Program Memory installed.



IN1 - Address decode that, when low, enables buffer M9 for data input to the microprocessor of TEST, SLAM, FIRE switches, and Trak Ball vertical and horizontal rate of turn.

IN2 - Address decode that, when low, enables buffer P10 for data input to the microprocessor of switch settings of DIP switch R10.



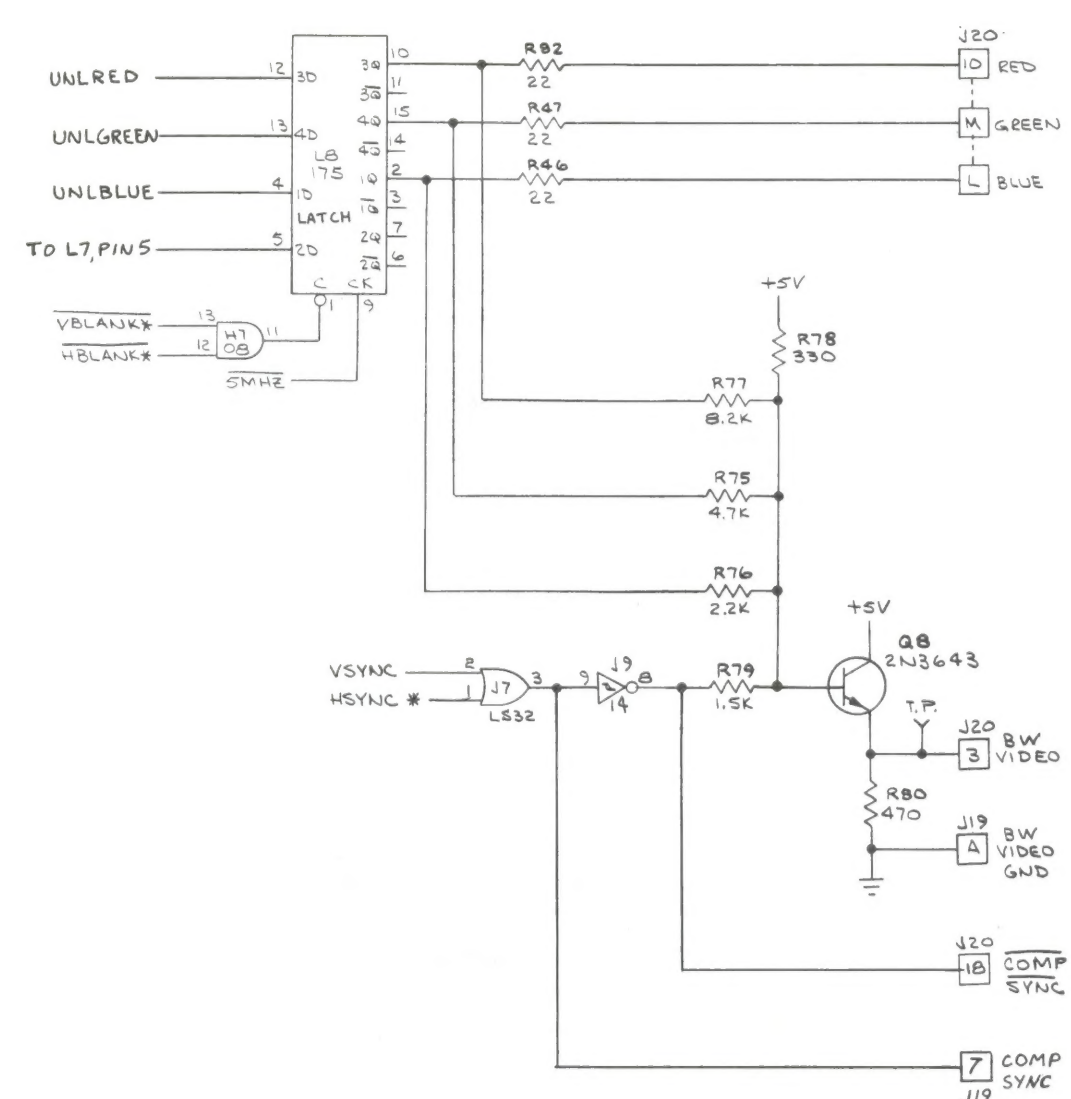
**Memory Map for Address Decoding Circuit,
Sheet 1, Side B**

MEMORY MAP																											
ADDRESS																	DATA										
HEXIDECIMAL	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
0000-01FF	0	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	512 Bytes of Working RAM	
0200-05FF	0	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	3rd-colorbit region of Screen RAM	
0600-063F	0	0	0	0	1	1	0	0	0	0	0	A	A	A	A	A		D	D	D	D	D	D	D	D	More Working RAM	
06FD-3FFF	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	2-colorbit region of Screen RAM	
4000-400F 4800	0	1	0	0	0	0	0	0	0	0	0	0	0	0	A	A		D	D	D	D	D	D	D	D	POKEY Ports	
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D							Right Coin Switch Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R		D						Center Coin Switch Input		
	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R			D					Left Coin Switch Input		
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R				D				D	1-player Start Switch Input	
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R					D			D	2-player Start Switch Input	
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R						D		D	2nd-player left Fire Switch Input (Cocktail Only)	
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R							D	D	2nd-player center Fire Switch Input (Cocktail Only)	
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R								D	D	2nd-player right Fire Switch Input (Cocktail Only)
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R		D	D						D	Horizontal TRAK BALL displacement if CTRLD latched high
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D						D	Vertical TRAK BALL displacement if CTRLD latched high
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W									D	Screen Flip
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W			D							Left Coin Counter Output
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W				D						Right Coin Counter Output
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W					D					Right Coin Counter Output
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W						D				2-Player Start LED Output
4900	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W								D		1-Player Start LED Output
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W								D		CTRLD - If low, read Switches. If high, read TRAK BALL
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D							D	VLANBK read
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	R			D						D
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R			D							SLAM Switch Input
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R				D						Horizontal TRAK BALL Direction Input
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R					D				D	Vertical TRAK BALL Direction Input
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R						D			D	1st-player left Fire Switch Input
4A00 4800-4B07	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R								D		1st-player center Fire Switch Input
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R								D		1st-player right Fire Switch Input
	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	R	D	D	D		D	D	D	D	D	Option Switch Inputs
	0	1	0	0	1	0	1	0	0	0	0	0	0	0	A	A	W					D	D	D	D	D	D
4C00	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W										Watchdog
4D00	0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	W										Interrupt Acknowledge
5000-7FFF	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	D	Program

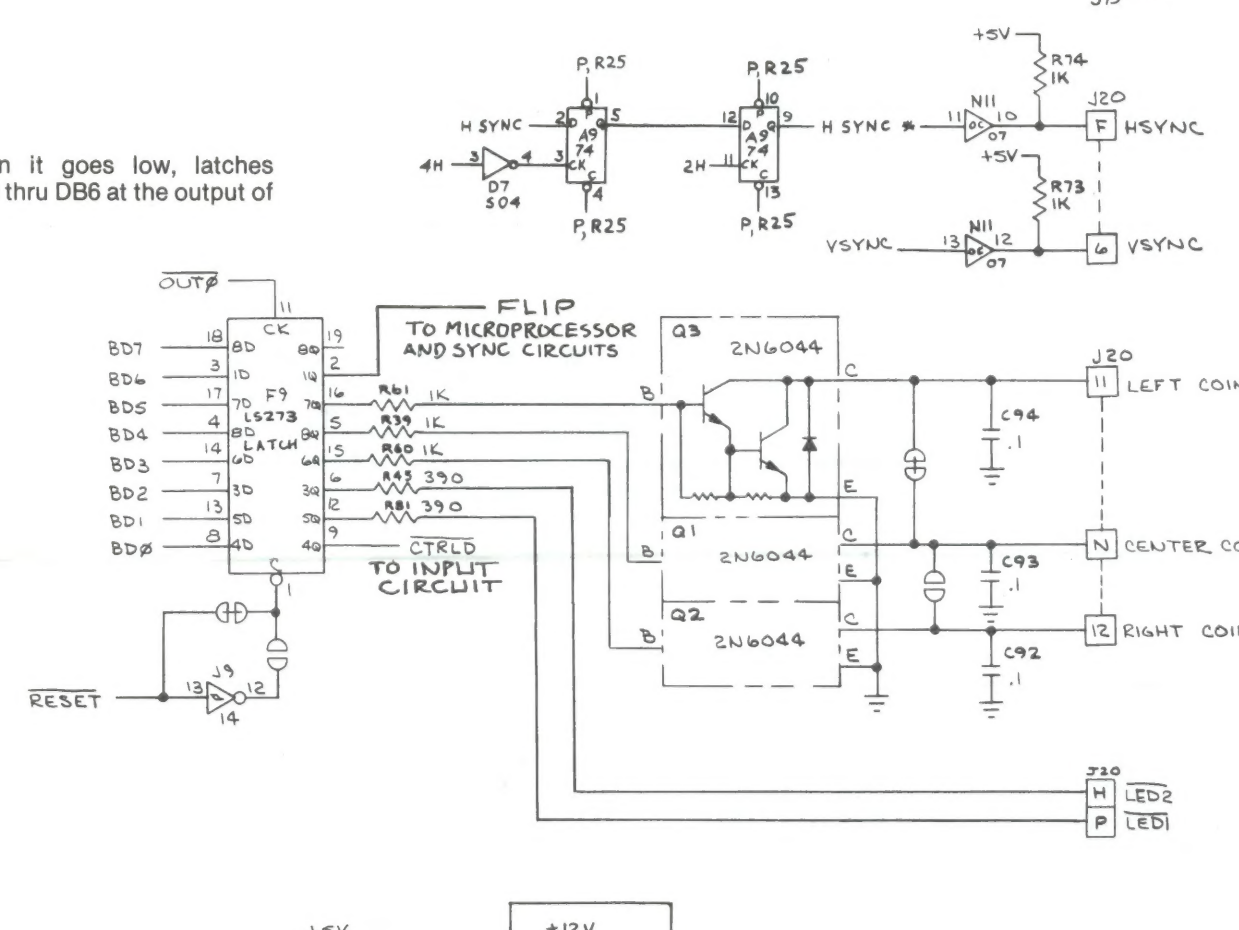
VTB CLKX (Vertical Trak Ball Clock) - Player 1 or player 2 vertical Trak Ball clock input to game PCB from vertical steering PCB of Trak Ball. Player 2 input is used only in Cocktail game, and game PCB must have -02 or higher Program Memory Installed.

VTB DIRX (Vertical Trak Ball Direction) - Player 1 or player 2 vertical Trak Ball direction input to game PCB from vertical steering PCB of Trak Ball. Player 2 input is used only in Cocktail game, and game PCB must have -02 or higher Program Memory Installed.

IN0 - Address decode that, when low, enables buffer L9 for data input to the microprocessor of COIN switches, START switches, player 2 FIRE switches (for Cocktail game only), or Trak Ball rate of turn information. If CTRLD is low, data is from switches. If high, Data is Trak Ball information.

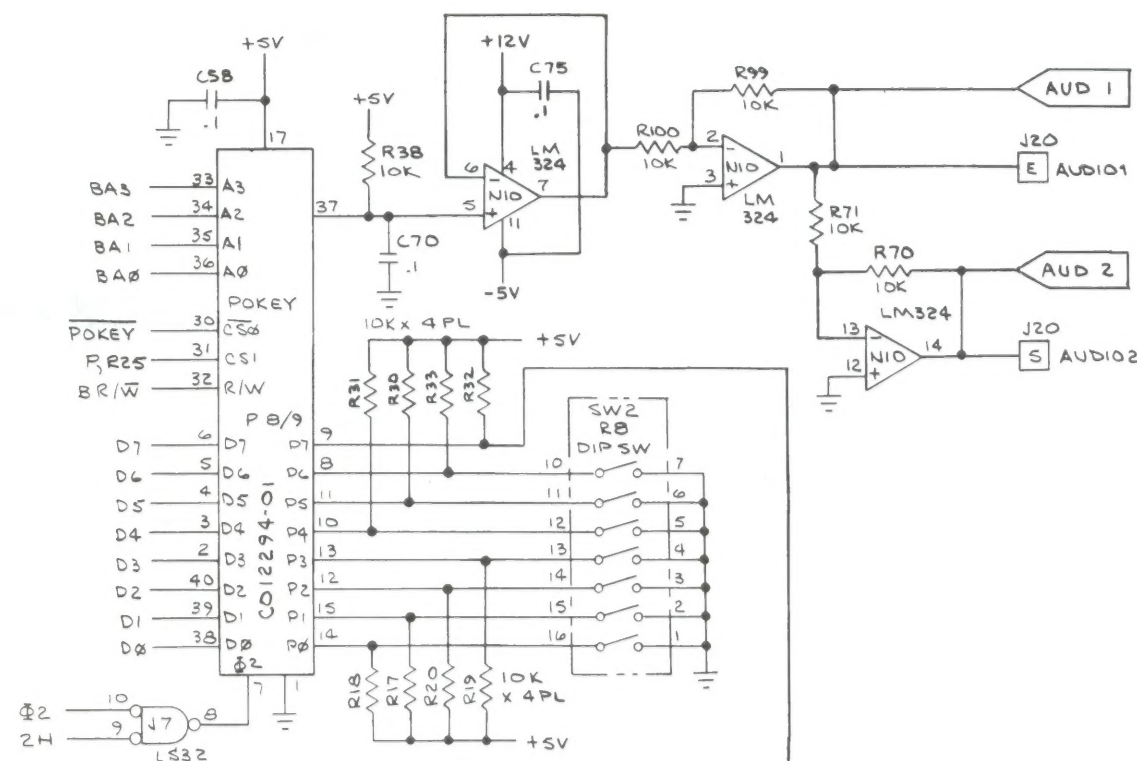


OUT0 - Address decode that, when it goes low, latches microprocessor-buffered data bits DB0 thru DB6 at the output of latch F9.



POKEY (*POKEY chip enable*) - Address decode that, when low, enables custom I/O POKEY chip N/PB/9 for data input or output. The POKEY chip works in conjunction with the microprocessor. It is the input port for DIP switch R8 and the audio output port. BR/W determines the direction of data flow as addressed by BA0 thru BA3.

BR/W (Buffered Read/Write) - Microprocessor-generated signal that, when high, allows microprocessor to read POKEY input data from DIP switch R8. When low, allows microprocessor to write to POKEY output.



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 A Warner Communications Company

Sheet 2, Side B

MISSILE COMMAND™

Input and Output Circuitry

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Sheet 2, Side B
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